

IN THE CLAIMS

Please amend the claims as follows:

Claims 1-20. (Canceled)

21. (Currently Amended) A system, comprising:

an Input/Output (I/O) control circuit to control transfer of data between a memory and an I/O device; and

a prefetch circuit to prefetch a data block into the memory in advance of a subsequent read made from the I/O device, wherein the data block is prefetched from a predicted address of the I/O device based on a preceding address associated with a previous read from the I/O device, and wherein the subsequent read is tracked to determine if the subsequent read reads from the predicted address, and wherein the prefetch circuit is adapted to ~~perform at least one of to~~ continue prefetching in response to the subsequent read, which is successful, and to stop prefetching in response to the subsequent read, which is unsuccessful.

22. (Previously Presented) The system of claim 21 further comprising, a state machine to adjust an additional predicted address associated with an additional subsequent read made from the I/O device based on whether the subsequent read reads from the predicted address.

23. (Previously Presented) The system of claim 21 wherein the prefetch circuit is included within the I/O control circuit.

24. (Previously Presented) The system of claim 21 wherein the prefetch circuit is an interface for a processor, the memory, and the I/O device.

25. (Currently Amended) A system, comprising:

an Input/Output (I/O) control circuit to control transfer of data between a memory and an I/O device; and

a prefetch circuit to prefetch a data block into the memory in advance of a subsequent read made from the I/O device, wherein the data block is prefetched from a predicted address of the I/O device based on a preceding address associated with a previous read from the I/O device, and wherein the subsequent read is tracked to determine if the subsequent read reads from the predicted address, and wherein the prefetch circuit is adapted to perform at least one of to continue prefetching in response to the subsequent read and to stop prefetching in response to the subsequent read, and ~~The system of claim 21 wherein the predicted address begins within the I/O device at a location of the preceding address plus a length of a preceding data block associated with the previous read plus 1.~~

26. (Previously Presented) The system of claim 21 wherein the prefetch circuit continues to prefetch additional data blocks associated with additional subsequent reads made from the I/O device at additional predicted addresses as long as the additional subsequent reads continues to at least partially match the additional predicted addresses.

27. (Previously Presented) The system of claim 26 wherein if the additional subsequent reads do not at least partially match the additional predicted addresses, then the prefetch circuit biases against prefetching and performs periodic checks to determine if biasing in favor of prefetching should resume.

28. (Currently Amended) A system, comprising:

a processor;

an Input/Output (I/O) device; and

a prefetch interface to prefetch data from the I/O device in advance of a request made by the processor for that data, wherein the prefetch interface predicts an address needed within the I/O device to satisfy the request, and wherein the prefetch interface tracks its performance and performs ~~at least one of~~, in response to success rates, ~~continues~~ continuing to prefetch for

additional data for favorable success rates and stops stopping prefetching for the additional data for unfavorable success rates.

29. (Previously Presented) The system of claim 28 wherein the prefetch interface adjusts subsequent predicted addresses associated with subsequent requests when at least a portion of the prefetched data satisfies the request.

30. (Previously Presented) The system of claim 28 wherein the prefetch interface is self-configurable to determine when to bias in favor of prefetching and when to bias against prefetching based on moving averages associated with the success rates.

31. (Previously Presented) The system of claim 30 wherein the prefetch interface includes a state machine that performs the tracking and self-configuration.

32. (Previously Presented) The system of claim 31 wherein the state machine includes a first state where prefetching takes place and a second state where prefetching is suspended.

33. (Currently Amended) A system, comprising:
a processor;
an Input/Output (I/O) device; and
a prefetch interface to prefetch data from the I/O device in advance of a request made by the processor for that data, wherein the prefetch interface predicts an address needed within the I/O device to satisfy the request, and wherein the prefetch interface tracks its performance and performs at least one of, in response to success rates, continues to prefetch for additional data and stops prefetching for the additional data, and wherein the prefetch interface is self-configurable to determine when to bias in favor of prefetching and when to bias against prefetching based on moving averages associated with the success rates, and the prefetch interface includes a state machine that performs the tracking and self-configuration, and wherein the state machine includes a first state where prefetching takes place and a second state where

prefetching is suspended and The system of claim 32 wherein the state machine includes a third state that biases towards prefetching and a fourth state that biases towards not prefetching.

34. (Previously Presented) A method, comprising:

prefetching a data block for a predicted address within Input/Output (I/O) device in advance of a read request made from a processor based on prior read requests made to the I/O device;

tracking a success rate of the predicted address when the request is made by the processor; and

adjusting the prefetching for subsequent predicted addresses based on the success rate in advance of subsequent read requests made by the processor, and wherein prefetching is not performed if the success rate includes two or more successive failures.

35. (Previously Presented) The method of claim 34 further comprising biasing in favor of not performing the prefetching when the tracking demonstrates an unacceptable success rate.

36. (Previously Presented) The method of claim 34 further comprising biasing in favor of the prefetching when the tracking demonstrates an acceptable success rate.

37. (Previously Presented) The method of claim 34 wherein prefetching further includes predicting the predicted address based on a prior read request made by the processor.

38. (Previously Presented) The method of claim 37 wherein the predicting further includes using a prior address within the I/O device associated with the prior read request to predict the predicted address.

39. (Previously Presented) The method of claim 34 wherein the tracking further includes defining the success rate to include partial success where at least a portion of the prefetched data block satisfies the read request.

40. (Previously Presented) The method of claim 34 wherein the adjusting further includes processing a state machine to bias in favor of performing the prefetching or to bias against the prefetching.